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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,535	10/03/2003	Alexander I. Korobkov	P-9644	1312

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EXAMINER	
PATEL, SHAMBHAVI K	
ART UNIT	**PAPER NUMBER**
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,535	KOROBKOV, ALEXANDER I.	
	Examiner	Art Unit	
	Shambhavi Patel	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/03/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-68 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-15, and 17-68 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted step is the calculation of the clock skew based on the placement of the clock sources. Thus, though the necessary steps for predicting the clock skew are completed (placing clock sources throughout the design based on whether them maximum, intermediate, or minimum clock skew is to be computed), the clock skew itself is never calculated.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1, 17, 18, 20, 21, 35, 51, 52, 55, 65, 66, and 68 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The examiner asserts that the current state of the claim language is such that a reasonable interpretation of the claims would not result in any concrete or tangible products. After the locations of the clock sources have been determined, the claim cites that placed onto the design. However, there is no evidence in the claims or specification that placing the clock sources onto the design produces a tangible result.

Claim 21 is directed to a clock skew prediction tool. The specification cites that the tool may be a computer program of a set of computer program modules of running on a computer system [0039]. Thus, the claimed invention is software only, and it lacks the necessary hardware to enable any functionality to be realized.

Allowable Subject Matter

Claims 1-68 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph and 35 U.S.C. 101, set forth in this Office action.

The following is an examiner's statement of reasons for allowance:

Regarding claims 1, 21, 35 and 55:

Applicant is disclosing a method, apparatus, and program storage device for predicting a clock skew for an incomplete integrated circuit design including at least one clock design for routing a clock signal. This has been disclosed in the prior art of record.

The prior art of record does not disclose the method, apparatus and program storage device wherein there is an option to determine whether the minimum skew, maximum skew, or intermediate skew is to be determined; if a minimum clock skew is to be determined, placing clock sources with a first predetermined minimum distance between adjacent clock sources; if a maximum clock skew is to be determined, placing a clock source on a first clock design figure having a largest size in the first layer, such that the clock source has a largest distance from a via to a lower layer; if an intermediate clock skew is to be determined, placing clock source locations on intersections between the clock design figure and a virtual clock grid created for the metal layer.

The closest prior art uncovered during examination teaches certain limitations of the claimed invention as follows:

US Patent 6,496,966 issued to Barney et al.: Teaches clock regions located symmetrically along each of the clock trunk lines (column 4 lines 54-58), but does not disclose grid-like lines.

US Patent 6,934,924 (issued to Paul et al.) and **US Patent Application Publication 2003/0043936** (Forbes): Teaches using a grid structure to place the top level clock (*Paul*: column 6 lines 11-13; *Forbes*: [0007]), but does not disclose a predetermined offset from a design

boundary from the grid, and does not disclose placing the clock at the intersection of the clock design figure and the clock grid.

US Patent 6,337,375 (issued to Block et al.): Teaches using a clock grid to determine the location of clock sources and route the signals between the sources (column 4 lines 24-41), but does not disclose multiple clock sources on multiple levels.

US Patent 5,866,924 (issued to Zhu): Teaches connecting a source to the sink that is determined to be the furthest distance (column 5 lines 14-17) from the source, but does not disclose the option of determining the minimum, maximum, or intermediate skew.

Independent claim 35 further uses "means for" language and is given deference in view of In re Donaldson and interpreted in view of 35 U.S.C. 112 paragraph 6. The "means for" language and the limitations related thereto of claim 35 are interpreted within the scope of enablement as provided within the relative embodiment provided within applicant's specification. In particular, the specific means for limitations as recited in the claims is interpreted as defined by the specifications as follows:

means for selecting a first metal layer ([0019] – [0020])

means for placing clock source locations on the clock design figure in accordance with a first predetermined minimum distance between adjacent clock source locations ([0020])

means for placing a clock source location on a first clock design figure having a largest size in the first layer, such that the clock source location has a largest distance from a via to a lower layer ([0020])

means for placing clock source locations on intersections between the clock design figure and a virtual clock grid created for the first metal layer ([0020])

The closest prior art, Barney (US Patent 6,496,966), Paul (US Patent 6,934,924), Forbes (US Patent Application Publication 2003/0043936), Block (US Patent 6,337,375), and Zhu (US Patent 5,866,924), either singularly or in combination, fail to anticipate or render the limitations above obvious. Dependent claims 2-16, 22-34, 36-50, and 56-64 are deemed allowable as depending from independent claims 1, 21, 35, and 55 respectively.

Regarding claims 17, 51, and 65:

Applicant is disclosing a method, apparatus, and product storage device for determining a clock skew for an incomplete integrated circuit design including at least one clock design figure for routing a clock signal. This is disclosed in the prior art made of record.

The prior art of record does not disclose the method, apparatus, and program storage device wherein a clock source is iteratively placed on successive metal layers with a first predetermined minimum distance between adjacent clock source locations if the clock design figures in the successive layers are not connected to a clock design figure in an upper metal layer.

The closest prior art uncovered during examination teaches certain limitations of the claimed invention as follows:

US Patent 6,934,924 (issued to Paul et al.) and **US Patent Application Publication 2003/0043936** (Forbes): Teaches using a grid structure to place the top-level clock (*Paul*: column 6 lines 11-13; *Forbes*: [0007]). Therefore, the clocks are connected to each other according to the distance between the grid lines, which are predetermined and symmetric. However, the distance between the clock sources is not necessarily predetermined, symmetric, or minimal because there is no indication in either of the prior art documents that the clock sources are placed in a particular and even pattern. Also, the art does not disclose iteratively placing clock sources on different metal layers based on their connectivity status.

US Patent 6,496,966 issued to Barney et al.: Teaches clock regions located symmetrically along each of the clock trunk lines (column 4 lines 54-58), but does not disclose grid-like lines. Also, the art does not disclose iteratively placing clock sources on different metal layers based on their connectivity status.

US Patent 5,912,820 issued to Kerzman et al.: Teaches placing clock drivers symmetrically and evenly along the circuit die (column 5 lines 45-51), but does not disclose the use of a virtual clock grid, or for repeating the process along multiple layers (if drivers on successive layers are not already connected to the top level clock).

Independent claim 51 further uses "means for" language and is given deference in view of In re Donaldson and interpreted in view of 35 U.S.C. 112 paragraph 6. The "means for" language and the limitations related thereto of claim 35 are interpreted within the scope of enablement as provided within the relative embodiment provided within applicant's

specification. In particular, the specific means for limitations as recited in the claims is interpreted as defined by the specifications as follows:

means for selecting a first metal layer ([0019] – [0020])

means for placing clock source locations in accordance with a predetermined minimum distance ([0020])

means for selecting a second metal layer ([0025])

means for determining if the clock design figure in the second metal layer is connected to a clock design figure in an upper metal layer ([0024]-[0025])

means for placing clock source locations on the clock design figure in the second metal layer in accordance with a second predetermined minimum distance between adjacent clock source locations ([0025])

means for iteratively executing said means for selecting a second metal layer, said means for determining, and said means for placing clock source locations in the second metal layer until all of the metal layers including at least one clock design figure are processed ([0024] – [0025])

The closest prior art, Barney (US Patent 6,496,966), Paul (US Patent 6,934,924), Forbes (US Patent Application Publication 2003/0043936), and Kerzman (US Patent 5,912,820), either singularly or in combination, fail to anticipate or render the limitations above obvious.

Regarding claims 18, 52, and 66:

Applicant is disclosing a method, apparatus, and program storage device for predicting a clock skew for an incomplete integrated circuit design including at least one clock design for routing a clock signal. This has been disclosed in the prior art of record.

The prior art of record does not disclose the method, apparatus, and program storage device wherein the first and second clock design figures chosen have the largest size, and placing said first and second clock sources such that the clock source location has a largest distance from a via to a lower layer. The prior art of record also does not teach iteratively repeating the selection, and placement of the second clock design figures.

The closest prior art uncovered during examination teaches certain limitations of the claimed invention as followed:

US Patent 5,866,924 issued to Zhu: Teaches repeatedly connected clock sources to the sink that is the furthest distance away (column 5 lines 14-16; column 6 lines 37-38). However, the distance is measured by using the "Manhattan" distance or "Euclidean" distance (column 5 lines 1-14), and does not measure the distance across metal layers.

US Patent 5,912,820 issued to Kerzman: Teaches minimizing the clock skew of an integrated circuit design by symmetrically and evenly placing clock drivers throughout the circuit, but does not disclosing measuring and accounting for the distance between clock sources and lower layers, or the size of the clock drivers.

Independent claim 52 further uses "means for" language and is given deference in view of In re Donaldson and interpreted in view of 35 U.S.C. 112 paragraph 6. The "means for" language and the limitations related thereto of claim 35 are interpreted within the scope of

enablement as provided within the relative embodiment provided within applicant's specification. In particular, the specific means for limitations as recited in the claims is interpreted as defined by the specifications as follows:

means for selecting a first metal layer including at least one clock design figure ([0019] – [0020])

means for selecting a first clock design figure having a largest size in the first metal layer ([0022], [0024])

means for placing a clock source location on the first clock design figure such that the clock source location has a largest distance from a via to a lower layer ([0022] – ([0023])

means for selecting a second clock design figure having a next largest size in the first metal layer ([0024])

means for determining if the second clock design figure is connected to an already processed clock design figure ([0024])

The closest prior art, Kerzman (US Patent 5,912,820), and Zhu (US Patent No. 5,866,924), either singularly or in combination, fail to anticipate or render the limitations above obvious. Dependent claims 19, 53, and 67 are deemed allowable as depending from independent claims 18, 51, and 66 respectively.

means for placing a clock source location on the second clock design figure such that the clock source location has a largest distance from a via to a lower layer ([0024])

means for iteratively executing said means for selecting a second clock design figure, said means for determining, and said means for placing a clock source location on the second clock design figure until all of the clock design figures in the first metal layer are processed ([0025])

Regarding claims 20, 54, and 68:

Applicant is disclosing a method, apparatus, and product storage device for determining a clock skew for an incomplete integrated circuit design including at least one clock design figure for routing a clock signal. This is disclosed in the prior art made of record.

The prior art of record does not disclose the method, apparatus, and program storage device wherein the virtual clock grid has a predetermined offset from a design boundary; placing clock source locations on intersections between the clock design figures and the virtual clock grid; repeating the above process for successive metal layers.

The closest prior art uncovered during examination teaches certain limitations of the claimed invention as follows:

US Patent 6,934,924 (issued to Paul et al.) Teaches using a grid structure to place the top-level clock (*Paul*: column 6 lines 11-13; *Forbes*: [0007]). Therefore, the clocks are connected to each other according to the distance between the grid lines, which are predetermined and symmetric. However, the distance between the clock sources is not necessarily predetermined, symmetric, or minimal because there is no indication in either of the prior art documents that the clock sources are placed in a particular and even pattern. Also, the art does not disclose iteratively placing clock sources on different metal layers based on their connectivity status.

US Patent No. 5,866,924 (Forbes): Teaches connected all sinks to a clock source in the integrated circuit design (column 6 lines 26-44). However, this process is only taught for one metal layer.

Independent claim 54 further uses "means for" language and is given deference in view of In re Donaldson and interpreted in view of 35 U.S.C. 112 paragraph 6. The "means for" language and the limitations related thereto of claim 35 are interpreted within the scope of enablement as provided within the relative embodiment provided within applicant's specification. In particular, the specific means for limitations as recited in the claims is interpreted as defined by the specifications as follows:

means for selecting a first metal layer including at least one clock design figure ([0019] – [0020])

means for creating a virtual clock grid for the first metal layer, the virtual clock grid having a predetermined offset from a design boundary and a predetermined pitch between grid lines ([0032] – [0036])

means for placing clock source locations on intersections between the clock design figure and the virtual clock grid ([0032] – [0036])

means for selecting a second metal layer including at least one clock design figure ([0032] – [0036])

means for creating a second virtual clock grid for the second metal layer, the second virtual clock grid having a second predetermined offset from a design boundary and a second predetermined pitch ([0032] – [0036])

means for determining if the clock design figure in the second metal layer is connected to a clock design figure in an upper metal layer ([0032] – [0036])

means for placing clock source locations on intersections between the clock design figure in the second metal layer and the second virtual clock grid, if the clock design figure in the second metal layer does not have a connection to a clock design figure in an upper metal layer ([0032] – [0036])

means for iteratively executing said means for selecting a second metal layer, said means for creating a second virtual clock grid, said means for determining, and means for said placing clock source locations in the second metal layer until all of the clock design figures have at least one clock source location provided therein or a connection to a clock design figure in an upper metal layer ([0032] – [0036])

The closest prior art, Kerzman (US Patent 5,912,820), and Zhu (US Patent No. 5,866,924), either singularly or in combination, fail to anticipate or render the limitations above obvious.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is 571 272 5877. The examiner can normally be reached on 7:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shambhavi Patel
Examiner
Art Unit 2128

SP

KAMINI SHAH
SUPERVISORY PATENT EXAMINER